National Semiconductor

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LM94
TruTherm™ Hardware Monitor with PI Loop Fan Control for Server Management

1.0 General Description

The LM94 hardware monitor has a two wire digital interface compatible with SMBus 2.0. Using a ΣΔ ADC, the LM94 measures the temperature of four remote diode connected transistors as well as its own die and 16 power supply voltages. The LM94 has new TruTherm technology that supports precision thermal diode measurements of processors on sub-micron processes.

To set fan speed, the LM94 has two PWM outputs that are each controlled by up to six temperature zones. The fan-control algorithm can be based on a lookup table, PI (proportional/integral) control loop, or a combination of both. The LM94 includes digital filters that can be invoked to smooth temperature readings for better control of fan speed such that acoustical noise is minimized. The LM94 has four tachometer inputs to measure fan speed. Limit and status registers for all measured values are included.

The LM94 builds upon the functionality of previous motherboard server management ASICs, such as the LM93. It also adds measurement and control support for dynamic Vccp monitoring for VRD10/11 and $\overline{\text{PROCHOT}}$. It is designed to monitor a dual processor Xeon class motherboard with a minimum of external components.

2.0 Features

- 8-bit ΣΔ ADC
- Monitors 16 power supplies
- Monitors 4 remote thermal diodes and 2 LM60
- New TruTherm technology support for precision thermal diode measurements
- Internal ambient temperature sensing
- Programmable autonomous fan control based on temperature readings with fan boost support
- Fan boost support on tachometer limit error event
- Fan control based on 13-step lookup table or PI Control Loop or combination of both
- PI fan control loop supports Tcontrol
- Temperature reading digital filters
- 0.5˚C digital temperature sensor resolution
- 0.0625˚C filtered temperature resolution for fan control
- 2 PWM fan speed control outputs
- 4 fan tachometer inputs
- Dual processor thermal throttling ($\overline{\text{PROCHOT}}$) monitoring
- Dual dynamic VID monitoring (6/7 VIDs per processor) supports VRD10.2/11
- 8 general purpose I/Os:
  - — 4 can be configured as fan tachometer inputs
  - — 2 can be configured to connect to processor $\overline{\text{THERMTRIP}}$
  - — 2 are standard GPIOs that could be used to monitor $\overline{\text{IERR}}$ signal
- 2 general purpose inputs that can be used to monitor the 7th VID signal for VRD11
- Limit register comparisons of all monitored values
- 2-wire serial digital interface, SMBus 2.0 compliant
  - — Supports byte/block read and write
  - — Selectable slave address (tri-level pin selects 1 of 3 possible addresses)
  - — $\overline{\text{ALERT}}$ output supports interrupt or comparator modes
- 2.5V reference voltage output
- 56-pin TSSOP package
- XOR-tree test mode

3.0 Key Specifications

■ Voltage Measurement Accuracy	±2% FS (max)
■ Temperature Resolution	9-bits, 0.5˚C
■ Temperature Sensor Accuracy	±2.5 ˚C (max)
■ Temperature Range:	
— LM94 Operational	0˚C to +85˚C
— Remote Temp Accuracy	0˚C to +125˚C
■ Power Supply Voltage	+3.0V to +3.6V
■ Power Supply Current	1.6 mA

4.0 Applications

- Servers
- Workstations
- Multi-processor based equipment

5.0 Ordering Information

Order Number	NS Package Number	Transport media
LM94CIMT	MTD56	34 units in rail
LM94CIMTX	MTD56	1000 units in tape-and-reel

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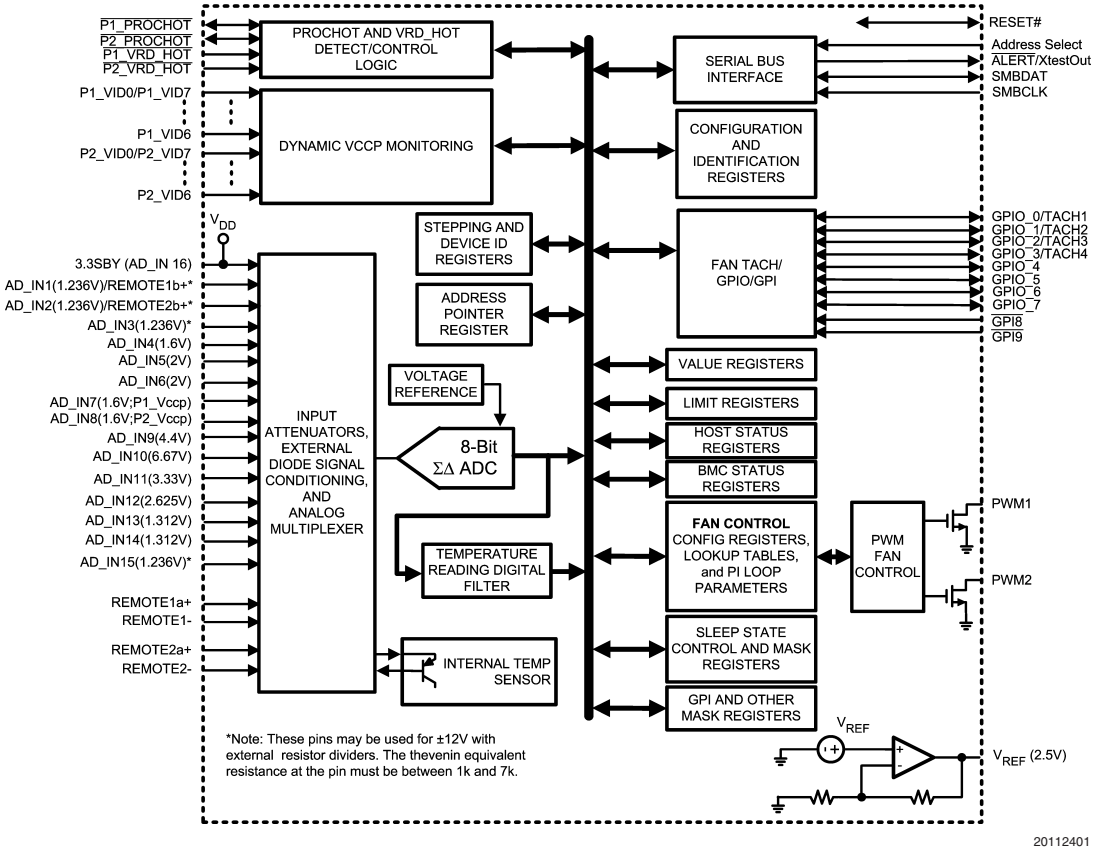
6.0 Block Diagram

The block diagram of LM94 hardware is illustrated below. The hardware implementation is a single chip ASIC solution.



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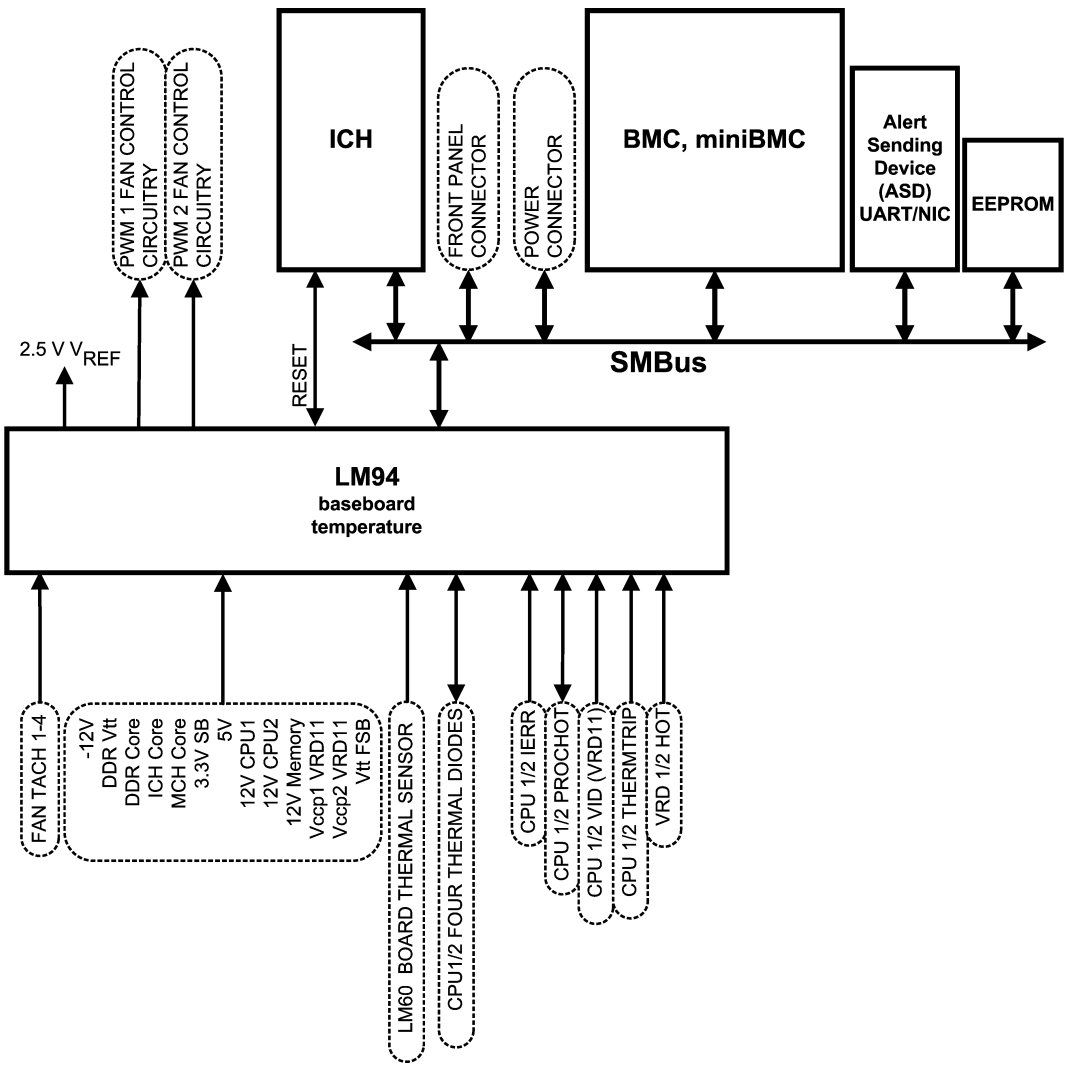
7.0 Application

Baseboard management of a dual processor server. Two LM94s may be required to manage a quad processor board. The system diagram below shows a dual processor server

2 Way Xeon Server Management



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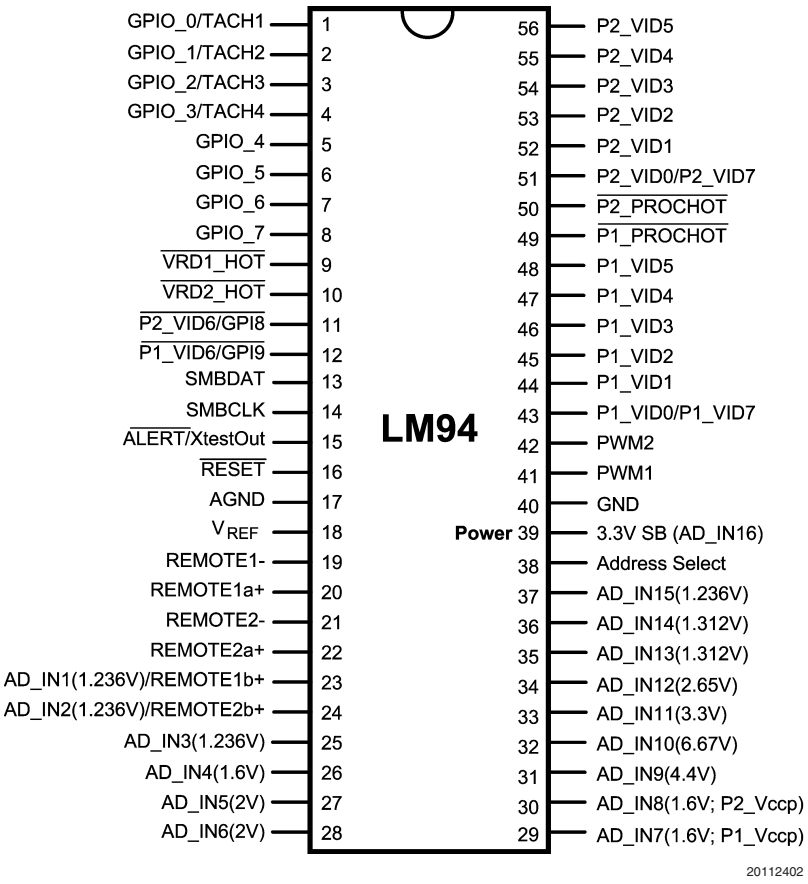
8.0 Connection Diagram

56 Pin TSSOP



NS Package MTD56
Top View
NS Order Numbers:
LM94CIMT (34 units per rail), or
LM94CIMTX (1000 units per tape-and-reel)

9.0 Pin Descriptions

Symbol	Pin #	Type	Function
GPIO_0/TACH1	1	Digital I/O (Open-Drain)	Can be configured as fan tach input or a general purpose open-drain digital I/O.
GPIO_1/TACH2	2	Digital I/O (Open-Drain)	Can be configured as fan tach input or a general purpose open-drain digital I/O.
GPIO_2/TACH3	3	Digital I/O (Open-Drain)	Can be configured as fan tach input or a general purpose open-drain digital I/O.
GPIO_3/TACH4	4	Digital I/O (Open-Drain)	Can be configured as fan tach input or a general purpose open-drain digital I/O..
GPIO_4 / $\overline{\text{P1\_THERMTRIP}}$	5	Digital I/O (Open-Drain)	A general purpose open-drain digital I/O. Can be configured to monitor a CPU's $\overline{\text{THERMTRIP}}$ signal to mask other errors. Supports TTL input logic levels and AGTL compatible input logic levels.
GPIO_5 / $\overline{\text{P2\_THERMTRIP}}$	6	Digital I/O (Open-Drain)	A general purpose open-drain digital I/O. Can be configured to monitor a CPU's $\overline{\text{THERMTRIP}}$ signal to mask other errors. Supports TTL input logic levels and AGTL compatible input logic levels.
GPIO_6	7	Digital I/O (Open-Drain)	Can be used to detect the state of CPU1 $\overline{\text{IERR}}$ or a general purpose open-drain digital I/O. Supports TTL input logic levels and AGTL compatible input logic levels.
GPIO_7	8	Digital I/O (Open-Drain)	Can be used to detect the state of CPU2 $\overline{\text{IERR}}$ or a general purpose open-drain digital I/O. Supports TTL input logic levels and AGTL compatible input logic levels.
$\overline{\text{VRD1\_HOT}}$	9	Digital Input	CPU1 voltage regulator $\overline{\text{HOT}}$. Supports TTL input logic levels and AGTL compatible input logic levels.
$\overline{\text{VRD2\_HOT}}$	10	Digital Input	CPU2 voltage regulator $\overline{\text{HOT}}$. Supports TTL input logic levels and AGTL compatible input logic levels.
$\overline{\text{P2\_VID6}}$/$\overline{\text{GPI8}}$	11	Digital Input	CPU2 VID6 input. Could also be used as a general purpose input to trigger an error event. Supports TTL input logic levels and AGTL compatible input logic levels.
$\overline{\text{P1\_VID6}}$/$\overline{\text{GPI9}}$	12	Digital Input	CPU1 VID6 input. Could also be used as a general purpose input to trigger an error event. Supports TTL input logic levels and AGTL compatible input logic levels.
SMBDAT	13	Digital I/O (Open-Drain)	Bidirectional System Management Bus Data. Output configured as 5V tolerant open-drain. SMBus 2.0 compliant.
SMBCLK	14	Digital Input	System Management Bus Clock. Driven by an open-drain output, and is 5V tolerant. SMBus 2.0 Compliant.
$\overline{\text{ALERT}}$/XtestOut	15	Digital Output (Open-Drain)	Open-drain $\overline{\text{ALERT}}$ output used in an interrupt driven system to signal that an error event has occurred. Masked error events do not activate the $\overline{\text{ALERT}}$ output. When in XOR tree test mode, functions as XOR Tree output.
$\overline{\text{RESET}}$	16	Digital I/O (Open-Drain)	Open-drain reset output when power is first applied to the LM94. Used as a reset for devices powered by 3.3V stand-by. After reset, this pin becomes a reset input. If this pin is not used, connection to an external resistive pull-up is required to prevent LM94 malfunction.
AGND	17	GROUND Input	Analog Ground. Digital ground and analog ground need to be tied together at the chip then both taken to a low noise system ground. A voltage difference between analog and digital ground may cause erroneous results.
V_{REF}	18	Analog Output	2.5V used for external ADC reference, or as a V_{REF} reference voltage

9.0 Pin Descriptions (Continued)

Symbol	Pin #	Type	Function
REMOTE1−	19	Remote Thermal Diode_1- Input (CPU 1 THERMDC)	This is the negative input (current sink) from both of the CPU1 thermal diodes. Connected to THERMDC pin of Pentium processor or the emitter of a diode connected MMBT3904 NPN transistor. Serves as the negative input into the A/D for thermal diode voltage measurements. A 100 pF capacitor is optional and can be connected between REMOTE1− and REMOTE1+.
REMOTE1a+	20	Remote Thermal Diode_1+ I/O (CPU1 THERMDA1)	This is a positive connection to the first CPU1 thermal diode. Serves as the positive input into the A/D for thermal diode voltage measurements. It also serves as a current source output that forward biases the thermal diode. Connected to THERMDA pin of Pentium processor or the base of a diode connected MMBT3904 NPN transistor. A 100 pF capacitor is optional and can be connected between REMOTE1− and each REMOTE1+.
REMOTE2−	21	Remote Thermal Diode_2 - Input (CPU2 THERMDC)	This is the negative input (current sink) from both of the CPU2 thermal diodes. Connected to THERMDC pins of Pentium processor or the emitter of a diode connected MMBT3904 NPN transistor. Serves as the negative input into the A/D for thermal diode voltage measurements. A 100 pF capacitor is optional and can be connected between REMOTE2− and each REMOTE2+.
REMOTE2a+	22	Remote Thermal Diode_2 + I/O (CPU2 THERMDA1)	This is a positive connection to the first CPU2 thermal diode. Serves as the positive input into the A/D for thermal diode voltage measurements. It also serves as a current source output that forward biases the thermal diode. Connected to THERMDA pin of Pentium processor or the base of a diode connected MMBT3904 NPN transistor. A 100 pF capacitor is optional and can be connected between REMOTE2− and REMOTE2+.
AD_IN1/REMOTE1b+	23	Analog Input (+12V1 or CPU1 THERMDA2)	Analog Input for +12V Rail 1 monitoring, for CPU1 voltage regulator. External attenuation resistors required such that 12V is attenuated to 0.927V for nominal ¾ scale reading. This pin may also serve as the second positive thermal diode input for CPU1.
AD_IN2/REMOTE2b+	24	Analog Input (+12V2 or CPU2 THERMDA2)	Analog Input for +12V Rail 2 monitoring, for CPU2 voltage regulator. External attenuation resistors required such that 12V is attenuated to 0.927V for nominal ¾ scale reading. This pin may also serve as the second positive thermal diode input for CPU2.
AD_IN3	25	Analog Input (+12V3)	Analog Input for +12V Rail 3, for Memory/3GIO slots. External attenuation resistors required such that 12V is attenuated to 0.927V for nominal ¾ scale reading.
AD_IN4	26	Analog Input (FSB_Vtt)	Analog input for 1.2V monitoring, nominal ¾ scale reading
AD_IN5	27	Analog Input (3GIO / PXH / MCH_Core)	Analog input for 1.5V monitoring, nominal ¾ scale reading
AD_IN6	28	Analog Input (ICH_Core)	Analog input for 1.5V monitoring, nominal ¾ scale reading
AD_IN7 (P1_Vccp)	29	Analog Input (CPU1_Vccp)	Analog input for +Vccp (processor voltage) monitoring.
AD_IN8 (P2_Vccp)	30	Analog Input (CPU2_Vccp)	Analog input for +Vccp (processor voltage) monitoring.
AD_IN9	31	Analog Input (+3.3V)	Analog input for +3.3V monitoring, nominal ¾ scale reading
AD_IN10	32	Analog Input (+5V)	Analog input for +5V monitoring silver box supply monitoring, nominal ¾ scale reading

9.0 Pin Descriptions (Continued)

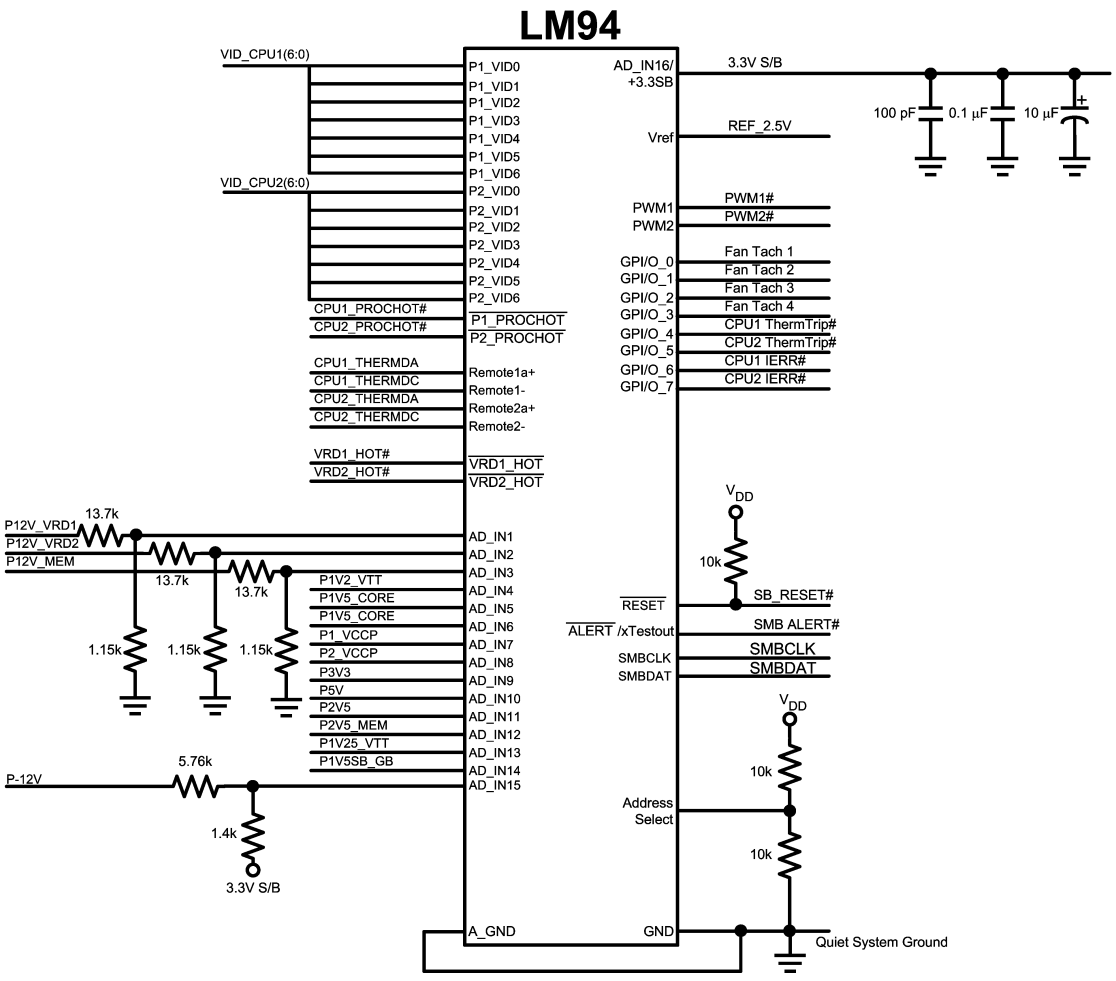
Symbol	Pin #	Type	Function
AD_IN11	33	Analog Input (SCSI_Core)	Analog input for +2.5V monitoring, nominal ¾ scale reading. This pin may also be used to monitor an analog temperature sensor such as the LM60, since readings from this input can be routed to the fan control logic.
AD_IN12	34	Analog Input (Mem_Core)	Analog input for +1.969V monitoring, nominal ¾ scale reading.
AD_IN13	35	Analog Input (Mem_Vtt)	Analog input for +0.984V monitoring, nominal ¾ scale reading.
AD_IN14	36	Analog Input (Gbit_Core)	Analog input for +0.984V S/B monitoring, nominal ¾ scale reading.
AD_IN15	37	Analog Input (-12V)	Analog input for -12V monitoring. External resistors required to scale to positive level. Full scale reading at 1.236V, , nominal ¾ scale reading. This pin may also be used to monitor an analog temperature sensor such as the LM60, since readings from this input can be routed to the fan control logic.
Address Select	38	3 level analog input	This input selects the lower two bits of the LM94 SMBus slave address.
3.3V SB (AD_IN16)	39	POWER (V_{DD}) +3.3V standby power	V_{DD} power input for LM94. Generally this is connected to +3.3V standby power. The LM94 can be powered by +3.3V if monitoring in low power states is not required, but power should be applied to this input before any other pins. This pin also serves as the analog input to monitor the 3.3V stand-by (SB) voltage. It is necessary to bypass this pin with a 0.1 µF in parallel with 100 pF. A bulk capacitance of 10 µF should be in the near vicinity. The 100 pF should be closest to the power pin.
GND	40	GROUND	Digital Ground. Digital ground and analog ground need to be tied together at the chip then both taken to a low noise system ground. A voltage difference between analog and digital ground may cause erroneous results.
PWM1	41	Digital Output (Open-Drain)	Fan control output 1.
PWM2	42	Digital Output (Open-Drain)	Fan control output 2
P1_VID0/P1_VID7	43	Digital Input	Voltage Identification signal from the processor. Supports TTL input logic levels and AGTL compatible input logic levels.
P1_VID1	44	Digital Input	Voltage Identification signal from the processor. Supports TTL input logic levels and AGTL compatible input logic levels.
P1_VID2	45	Digital Input	Voltage Identification signal from the processor. Supports TTL input logic levels and AGTL compatible input logic levels.
P1_VID3	46	Digital Input	Voltage Identification signal from the processor. Supports TTL input logic levels and AGTL compatible input logic levels.
P1_VID4	47	Digital Input	Voltage Identification signal from the processor. Supports TTL input logic levels and AGTL compatible input logic levels.
P1_VID5	48	Digital Input	Voltage Identification signal from the processor. Supports TTL input logic levels and AGTL compatible input logic levels.
$\overline{\text{P1\_PROCHOT}}$	49	Digital I/O (Open-Drain)	Connected to CPU1 $\overline{\text{PROCHOT}}$ (processor hot) signal through a bidirectional level shifter. Supports TTL input logic levels and AGTL compatible input logic levels.
$\overline{\text{P2\_PROCHOT}}$	50	Digital I/O (Open-Drain)	Connected to CPU2 $\overline{\text{PROCHOT}}$ (processor hot) signal through a bidirectional level shifter. Supports TTL input logic levels and AGTL compatible input logic levels.

9.0 Pin Descriptions (Continued)

Symbol	Pin #	Type	Function
P2_VID0/P2_VID7	51	Digital Input	Voltage Identification signal from the processor. Supports TTL input logic levels and AGTL compatible input logic levels.
P2_VID1	52	Digital Input	Voltage Identification signal from the processor. Supports TTL input logic levels and AGTL compatible input logic levels.
P2_VID2	53	Digital Input	Voltage Identification signal from the processor. Supports TTL input logic levels and AGTL compatible input logic levels.
P2_VID3	54	Digital Input	Voltage Identification signal from the processor. Supports TTL input logic levels and AGTL compatible input logic levels.
P2_VID4	55	Digital Input	Voltage Identification signal from the processor. Supports TTL input logic levels and AGTL compatible input logic levels.
P2_VID5	56	Digital Input	Voltage Identification signal from the processor. Supports TTL input logic levels and AGTL compatible input logic levels.

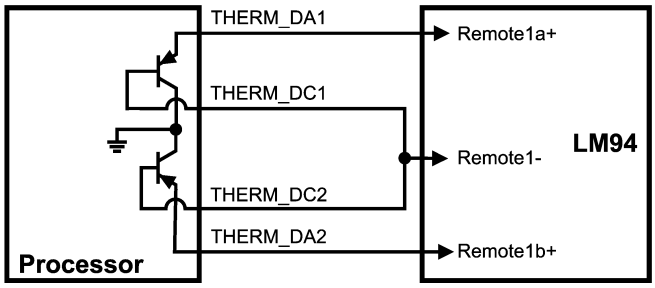
The over-score indicates the signal is active low (“Not”).

10.0 Recommended Implementation



Recommended implementation without thermal diode connections

10.0 Recommended Implementation (Continued)



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Note: 100 pF cap across each thermal diode is optional and should be placed close to the LM94, if used. The maximum capacitance between thermal diode pins is 300 pF.

Thermal diode recommended implementation

11.0 Functional Description

The LM94 provides 16 channels of voltage monitoring, 4 remote thermal diode monitors, an internal/local ambient temperature sensor, 2 $\overline{\text{PROCHOT}}$ monitors, 4 fan tachometers, 8 GPIOs, THERMTRIP monitor for masking error events, 2 sets of 7 VID inputs, an $\overline{\text{ALERT}}$ output and all the associated limit registers on a single chip, and communicates to the rest of the baseboard over the System Management Bus (SMBus). The LM94 also provides 2 PWM outputs and associated fan control logic for controlling the speed of system fans. There are two sets of fan control logic, a lookup table and a PI (proportional/integral) loop controller. The lookup table and PI controller are interactive, such that the fans run at the fastest required speed. Upon a temperature or fan tach error event, the PWM outputs may be programmed such that they automatically boost to 100% duty cycle. A timer is included that sets the minimum time that the fans are in the boost condition when activated by a fan tach error.

The LM94 incorporates National Semiconductor's TruTherm technology for precision "Remote Diode" readings of processors on 90nm process geometry or smaller. Readings from the external thermal diodes and the internal temperature sensor are made available as an 9-bit two's-complement digital value with the LSb representing 0.5˚C. Filtered temperature readings are available as a 12-bit two's-complement digital value with the LSb representing 0.0625˚C.

All but 4 of the analog inputs include internal scaling resistors. External scaling resistors are required for measuring ±12V. The inputs are converted to 8-bit digital values such that a nominal voltage appears at ¾ scale for positive voltages and ¼ scale for negative voltages. The analog inputs are intended to be connected to both baseboard resident VRDs and to standard voltage rails supplied by a SSI compliant power supply.

The LM94 has logic that ties a set of dynamically moving VID inputs to their associated Vccp analog input for real time window comparison fault determination. Voltage mapping for VRD10, VRD10 extended and VRD11are supported by the LM94. When VRD10 mode is selected GPI8 and GPI9 can be used to detect external error flags whose state is be reflected in the status registers.

Error events are captured in two sets of mirrored status registers (BMC Error Status Registers and Host Status Registers) allowing two controllers access to the status information without any interference.

The LM94's $\overline{\text{ALERT}}$ output supports interrupt mode or comparator mode of operation. The comparator mode is only functional for thermal monitoring.

The LM94 provides a number of internal registers, which are detailed in the register section of this document.

12.0 Please contact your local sales office for complete LM94 applications information.

13.0 Registers

13.1 REGISTER WARNINGS

In most cases, reserved registers and register bits return zero when read. This should not be relied upon, since reserved registers can be used for future expansion of the LM94 functions.

Some registers have "N/D" for their default value. This means that the power-up default of the register is not defined. In the case of value registers, care should be taken to ensure that software does not read a value register until the associated measurement function has acquired a measurement. This applies to temperatures, voltages, fan RPM, and $\overline{\text{PROCHOT}}$ monitoring.

13.0 Registers (Continued)

13.2 REGISTER SUMMARY TABLE

Register Key

Term	Description
N/D	Not Defined
N/A	Not Applicable
R	Read Only
R/W	Read or Write
RWC	Read or Write to Clear

Lock	Register Name	Address	Description
FACTORY REGISTERS			
x	XOR Test	00h	Used to set the XOR test tree mode
	SMBus Test	01h	SMBus read/write test register
	Reserved	02h-04h	
"REMOTE DIODE" MODE SELECT			
x	Transistor Mode Select	05h	Selects Diode Mode (default) or Transistor Mode for "Remote Diode" measurements
VALUE REGISTER SECTION 1			
	Zone 1b (CPU1 Diode b) Temp	06h	Measured value of remote thermal diode temperature channel 1b
	Zone 2b (CPU2 Diode b) Temp	07h	Measured value of remote thermal diode temperature channel 2b
	Zone 1b (CPU1 Diode b) Filtered Temp	08h	Filtered value of remote thermal diode temperature channel 1b
	Zone 2b (CPU2 Diode b) Fitlered Temp	09h	Filtered value of remote thermal diode temperature channel 2b
	PWM1 8-bit Duty Cycle Value	0Ah	8- bit value of the PWM1 duty cycle.
	PWM2 8-bit Duty Cycle Value	0Bh	8-bit value of the PWM2 duty cycle
HIGH RESOLUTION PWM OVERIDE REGISTERS			
x	PWM1 Duty Cycle Override (low byte)	0Ch	Lower byte of the high resolution PWM1 duty cycle register
x	PWM1 Duty Cycle Override (high byte)	0Dh	Upper byte of the high resolution PWM1 duty cycle register
x	PWM2 Duty Cycle Override (low byte)	0Eh	Lower byte of the high resolution PWM2 duty cycle register
x	PWM2 Duty Cycle Override (high byte)	0Fh	Upper byte of the high resolution PWM2 duty cycle register
EXTENDED RESOLUTION TEMPERATURE VALUE REGISTERS			
	Z1a_LSB	10h	Zone 1a (CPU1) extended resolution unfiltered temperature value register, least-significant byte
	Z1a_MSB	11h	Zone 1a (CPU1) extended resolution unfiltered temperature value register, most-significant byte
	Z1b_LSB	12h	Zone 1b (CPU1) extended resolution unfiltered temperature value register, least-significant-byte
	Z1b_MSB	13h	Zone 1b (CPU1) extended resolution unfiltered temperature value register, most-significant byte
	Z2a_LSB	14h	Zone 2a (CPU2) extended resolution unfiltered temperature value register, least-significant-byte
	Z2a_MSB	15h	Zone 2a (CPU2) extended resolution unfiltered temperature value register, most-significant byte

13.0 Registers (Continued)

Lock	Register Name	Address	Description
EXTENDED RESOLUTION TEMPERATURE VALUE REGISTERS			
	Z2b_LSB	16h	Zone 2b (CPU2) extended resolution unfiltered temperature value register, least-significant-byte
	Z2b_MSB	17h	Zone 2b (CPU2) extended resolution unfiltered temperature value register, most-significant byte
	Z1a_F_LSB	18h	Zone 1a (CPU1) extended resolution filtered temperature value register, least-significant byte
	Z1a_F_MSB	19h	Zone 1a (CPU1) extended resolution filtered temperature value register, most-significant byte
	Z1b_F_LSB	1Ah	Zone 1b (CPU1) extended resolution filtered temperature value register, least-significant-byte
	Z1b_F_MSB	1Bh	Zone 1b (CPU1) extended resolution filtered temperature value register, most-significant byte
	Z2a_F_LSB	1Ch	Zone 2a (CPU2) extended resolution filtered temperature value register, least-significant-byte
	Z2a_F_MSB	1Dh	Zone 2a (CPU2) extended resolution filtered temperature value register, most-significant byte
	Z2b_F_LSB	1Eh	Zone 2b (CPU2) extended resolution filtered temperature value register, least-significant-byte
	Z2b_F_MSB	1Fh	Zone 2b (CPU2) extended resolution filtered temperature value register, most-significant byte
	Z3_LSB	20h	Zone 3 (Internal) extended resolution temperature value register, least-significant byte
	Z3_MSB	21h	Zone 3 (Internal) extended resolution temperature value register, least-significant byte
	Z4_LSB	22h	Zone 4 (External Digital) extended resolution temperature value register, most-significant byte
	Z4_MSB	23h	Zone 4 (External Digital) extended resolution temperature value register, least-significant byte
	Reserved	24h-30h	
PI LOOP AND FAN CONTROL SETUP REGISTERS			
x	Temperature Source Select	31h	Selects the temperature source for some temperature zones.
x	PWM Filter Settings	32h	Sets the IIR filter coefficients for the PWM outputs for low resolution sources
x	PWM1 Filter Shutoff Threshold	33h	PWM1 Filter Shutoff Threshold
x	PWM2 Filter Shutoff Threshold	34h	PWM2 Filter Shutoff Threshold
x	PI/LUT Fan Control Bindings	35h	PI/LUT fan control binding configuration
x	PI Controller Minimum PWM and Hysteresis	36h	PI Controller Minimum PWM and Hysteresis settings
x	Zone 1 Tcontrol	37h	Zone 1 (CPU1) PI Controller Target Temperature (Tcontrol)
x	Zone 2 Tcontrol	38h	Zone 2 (CPU2) PI Controller Target Temperature (Tcontrol)
x	Zone 1 Toff	39h	Zone 1 (CPU1) PI Controller Off Temperature (Toff)
x	Zone 2 Toff	3Ah	Zone 2 (CPU2) PI Controller Off Temperature (Toff)
x	P Coefficient	3Bh	PI controller proportional coefficient
x	I Coefficient	3Ch	PI controller integral coefficient
x	PI Exponents	3Dh	PI controller coefficient exponents
DEVICE IDENTIFICATION REGISTERS			
	Manufacturer ID	3Eh	Contains manufacturer ID code

13.0 Registers (Continued)

Lock	Register Name	Address	Description
PI LOOP AND FAN CONTROL SETUP REGISTERS			
	Version/Stepping	3Fh	Contains code for major and minor revisions
BMC ERROR STATUS REGISTERS			
	B_Error Status 1	40h	BMC error status register 1
	B_Error Status 2	41h	BMC error register 2
	B_Error Status 3	42h	BMC error register 3
	B_Error Status 4	43h	BMC error register 4
	B_$\overline{\text{P1_PROCHOT}}$ Error Status	44h	BMC error register for $\overline{\text{P1\_PROCHOT}}$
	B_$\overline{\text{P2_PROCHOT}}$ Error Status	45h	BMC error register for $\overline{\text{P2\_PROCHOT}}$
	B_GPI Error Status	46h	BMC error register for GPIs
	B_Fan Error Status	47h	BMC error register for Fans
HOST ERROR STATUS REGISTERS			
	H_Error Status 1	48h	HOST error status register 1
	H_Error Status 2	49h	HOST error register 2
	H_Error Status 3	4Ah	HOST error register 3
	H_Error Status 4	4Bh	HOST error register 4
	H_$\overline{\text{P1_PROCHOT}}$ Error Status	4Ch	HOST error register for $\overline{\text{P1\_PROCHOT}}$
	H_$\overline{\text{P2_PROCHOT}}$ Error Status	4Dh	HOST error register for $\overline{\text{P2\_PROCHOT}}$
	H_GPI Error Status	4Eh	HOST error register for GPIs
	H_Fan Error Status	4Fh	HOST error register for Fans
VALUE REGISTERS SECTION 2			
	Zone 1a (CPU1) Temp	50h	Measured value of remote thermal diode temperature channel 1a
	Zone 2a (CPU2) Temp	51h	Measured value of remote thermal diode temperature channel 2a
	Zone 3 (Internal) Temp	52h	Measured temperature from on-chip sensor
	Zone 4 (External Digital) Temp	53h	Measured temperature from external temperature sensor
	Zone 1a (CPU1) Filtered Temp	54h	Filtered value of remote thermal diode temperature channel 1a
	Zone 2a (CPU2) Filtered Temp	55h	Filtered value of remote thermal diode temperature channel 2a
	AD_IN1 Voltage	56h	Measured value of AD_IN1
	AD_IN2 Voltage	57h	Measured value of AD_IN2
	AD_IN3 Voltage	58h	Measured value of AD_IN3
	AD_IN4 Voltage	59h	Measured value of AD_IN4
	AD_IN5 Voltage	5Ah	Measured value of AD_IN5
	AD_IN6 Voltage	5Bh	Measured value of AD_IN6
	AD_IN7 Voltage	5Ch	Measured value of AD_IN7
	AD_IN8 Voltage	5Dh	Measured value of AD_IN8
	AD_IN9 Voltage	5Eh	Measured value of AD_IN9
	AD_IN10 Voltage	5Fh	Measured value of AD_IN10
	AD_IN11 Voltage	60h	Measured value of AD_IN11
	AD_IN12 Voltage	61h	Measured value of AD_IN12
	AD_IN13 Voltage	62h	Measured value of AD_IN13
	AD_IN14 Voltage	63h	Measured value of AD_IN14
	AD_IN15 Voltage	64h	Measured value of AD_IN15
	AD_IN16 Voltage	65h	Measured value of AD_IN16 (V_{DD} 3.3V S/B)
	Reserved	66h	
	Current $\overline{\text{P1\_PROCHOT}}$	67h	Measured $\overline{\text{P1\_PROCHOT}}$ throttle percentage

13.0 Registers (Continued)

Lock	Register Name	Address	Description
VALUE REGISTERS SECTION 2			
	Average $\overline{\text{P1\_PROCHOT}}$	68h	Average $\overline{\text{P1\_PROCHOT}}$ throttle percentage
	Current $\overline{\text{P2\_PROCHOT}}$	69h	Measured $\overline{\text{P2\_PROCHOT}}$ throttle percentage
	Average $\overline{\text{P2\_PROCHOT}}$	6Ah	Average $\overline{\text{P2\_PROCHOT}}$ throttle percentage
	GPI State	6Bh	Current GPIO state
	P1_VID	6Ch	Current VID value of Processor 1
	P2_VID	6Dh	Current VID value of Processor 2
	FAN Tach 1 LSB	6Eh	Measured FAN Tach 1 LSB
	FAN Tach 1 MSB	6Fh	Measured FAN Tach 1 MSB
	FAN Tach 2 LSB	70h	Measured FAN Tach 2 LSB
	FAN Tach 2 MSB	71h	Measured FAN Tach 2 MSB
	FAN Tach 3 LSB	72h	Measured FAN Tach 3 LSB
	FAN Tach 3 MSB	73h	Measured FAN Tach 3 MSB
	FAN Tach 4 LSB	74h	Measured FAN Tach 4 LSB
	FAN Tach 4 MSB	75h	Measured FAN Tach 4 MSB
	Reserved	76h-77h	
TEMPERATURE LIMIT REGISTERS			
	Zone 1 (CPU1) Low Temp	78h	Low limit for external thermal diode temperature channel 1 (D1) measurement
	Zone 1 (CPU1) High Temp	79h	High limit for external thermal diode temperature channel 1 (D1) measurement
	Zone 2 (CPU2) Low Temp	7Ah	Low limit for external thermal diode temperature channel 2 (D2) measurement
	Zone 2 (CPU2) High Temp	7Bh	High limit for external thermal diode temperature channel 2 (D2) measurement
	Zone 3 (Internal) Low Temp	7Ch	Low limit for local temperature measurement
	Zone 3 (Internal) High Temp	7Dh	High limit for local temperature measurement
	Zone 4 (External Digital) Low Temp	7Eh	Low limit for external digital temperature sensor
	Zone 4 (External Digital) High Temp	7Fh	High limit for external digital temperature sensor
x	Fan Boost Temp Zone 1	80h	Zone 1 (CPU1) fan boost temperature
x	Fan Boost Temp Zone 2	81h	Zone 2 (CPU2) fan boost temperature
x	Fan Boost Temp Zone 3	82h	Zone 3 (Internal) fan boost temperature
x	Fan Boost Temp Zone 4	83h	Zone 4 (External Digital) fan boost temperature
	Zone1 and Zone 2 Hysteresis	84h	Zone 1 and Zone 2 hysteresis for limit comparisons
	Zone 3 and Zone 4 Hysteresis	85h	Zone 3 and Zone 4 hysteresis for limit comparisons
	Reserved	86h-8Dh	
ZONE 1b and 2b TEMPERATURE READING ADJUSTMENT REGISTERS			
	Zone 1b Temp Adjust	8Eh	Allows all Zone 1b temperature measurements to be adjusted by a programmable offset.
	Zone 2b Temp Adjust	8Fh	Allows all Zone 2b temperature measurements to be adjusted by a programmable offset.

13.0 Registers (Continued)

Lock	Register Name	Address	Description
OTHER LIMIT REGISTERS			
	AD_IN1 Low Limit	90h	Low limit for analog input 1 measurement
	AD_IN1 High Limit	91h	High limit for analog input 1 measurement
	AD_IN2 Low Limit	92h	Low limit for analog input 2 measurement
	AD_IN2 High Limit	93h	High limit for analog input 2 measurement
	AD_IN3 Low Limit	94h	Low limit for analog input 3 measurement
	AD_IN3 High Limit	95h	High limit for analog input 3 measurement
	AD_IN4 Low Limit	96h	Low limit for analog input 4 measurement
	AD_IN4 High Limit	97h	High limit for analog input 4 measurement
	AD_IN5 Low Limit	98h	Low limit for analog input 5 measurement
	AD_IN5 High Limit	99h	High limit for analog input 5 measurement
	AD_IN6 Low Limit	9Ah	Low limit for analog input 6 measurement
	AD_IN6 High Limit	9Bh	High limit for analog input 6 measurement
	AD_IN7 Low Limit	9Ch	Low limit for analog input 7 measurement
	AD_IN7 High Limit	9Dh	High limit for analog input 7 measurement
	AD_IN8 Low Limit	9Eh	Low limit for analog input 8 measurement
	AD_IN8 High Limit	9Fh	High limit for analog input 8 measurement
	AD_IN9 Low Limit	A0h	Low limit for analog input 9 measurement
	AD_IN9 High Limit	A1h	High limit for analog input 9 measurement
	AD_IN10 Low Limit	A2h	Low limit for analog input 10 measurement
	AD_IN10 High Limit	A3h	High limit for analog input 10 measurement
	AD_IN11 Low Limit	A4h	Low limit for analog input 11 measurement
	AD_IN11 High Limit	A5h	High limit for analog input 11 measurement
	AD_IN12 Low Limit	A6h	Low limit for analog input 12 measurement
	AD_IN12 High Limit	A7h	High limit for analog input 12 measurement
	AD_IN13 Low Limit	A8h	Low limit for analog input 13 measurement
	AD_IN13 High Limit	A9h	High limit for analog input 13 measurement
	AD_IN14 Low Limit	AAh	Low limit for analog input 14 measurement
	AD_IN14 High Limit	ABh	High limit for analog input 14 measurement
	AD_IN15 Low Limit	ACh	Low limit for analog input 15 measurement
	AD_IN15 High Limit	ADh	High limit for analog input 15 measurement
	AD_IN16 Low Limit	AEh	Low limit for analog input 16 measurement
	AD_IN16 High Limit	AFh	High limit for analog input 16 measurement
	$\overline{\text{P1\_PROCHOT}}$ User Limit	B0h	User settable limit for $\overline{\text{P1\_PROCHOT}}$
	$\overline{\text{P2\_PROCHOT}}$ User Limit	B1h	User settable limit for $\overline{\text{P2\_PROCHOT}}$
	Vccp1 Limit Offsets	B2h	VID offset values for window comparator for CPU1 Vccp (AD_IN7)
	Vccp2 Limit Offsets	B3h	VID offset values for window comparator for CPU2 Vccp (AD_IN8)
	FAN Tach 1 Limit LSB	B4h	FAN Tach 1 Limit LSB
	FAN Tach 1 Limit MSB	B5h	FAN Tach 1 Limit MSB
	FAN Tach 2 Limit LSB	B6h	FAN Tach 2 Limit LSB
	FAN Tach 2 Limit MSB	B7h	FAN Tach 2 Limit MSB
	FAN Tach 3 Limit LSB	B8h	FAN Tach 3 Limit LSB
	FAN Tach 3 Limit MSB	B9h	FAN Tach 3 Limit MSB
	FAN Tach 4 Limit LSB	BAh	FAN Tach 4 Limit LSB

13.0 Registers (Continued)

Lock	Register Name	Address	Description
OTHER LIMIT REGISTERS			
	FAN Tach 4 Limit MSB	BBh	FAN Tach 4 Limit MSB
SETUP REGISTERS			
	Special Function Control 1	BCh	Controls the hysteresis for voltage limit comparisons. Also selects filtered or unfiltered temperature usage for temperature limit comparisons and fan control.
	Special Function Control 2	BDh	Enables smart tach detection. Also selects 0.5˚C or 1.0˚C resolution for fan control.
x	GPI / VID Level Control	BEh	Control the input threshold levels for the P1_VIDx, P2_VIDx and GPIO_x inputs.
x	PWM Ramp Control	BFh	Controls the ramp rate of the PWM duty cycle when $\overline{\text{VRDx\_HOT}}$ is asserted, as well as the ramp rate when $\overline{\text{PROCHOT}}$ exceeds the user threshold.
x	Fan Boost Hysteresis (Zones 1/2)	C0h	Fan Boost Hysteresis for zones 1 and 2
x	Fan Boost Hysteresis (Zones 3/4)	C1h	Fan Boost Hysteresis for zones 3 and 4
x	Zones 1/2 Spike Smoothing Control	C2h	Configures Spike Smoothing for zones 1 and 2
x	LUT 1/2 MinPWM and Hysteresis	C3h	Controls MinPWM and hysteresis setting for LUT 1 and 2 auto-fan control
x	LUT 3/4 MinPWM and Hysteresis	C4h	Controls MinPWM and hysteresis setting for LUT 3 and 4 auto-fan control
	GPO	C5h	Controls the output state of the GPIO pins
	$\overline{\text{PROCHOT}}$ Control	C6h	Controls assertion of $\overline{\text{P1\_PROCHOT}}$ or $\overline{\text{P2\_PROCHOT}}$
	$\overline{\text{PROCHOT}}$ Time Interval	C7h	Configures the time window over which the $\overline{\text{PROCHOT}}$ inputs are measured
x	PWM1 Control 1	C8h	Controls PWM control source bindings.
x	PWM1 Control 2	C9h	Controls PWM override and output polarity
x	PWM1 Control 3	CAh	Controls PWM spin-up duration and duty cycle
x	PWM1 Control 4	CBh	Frequency control for PWM1.
x	PWM2 Control 1	CCh	Controls PWM control source bindings.
x	PWM2 Control 2	CDh	Controls PWM override and output polarity
x	PWM2 Control 3	CEh	Controls PWM spin-up duration and duty cycle
x	PWM2 Control 4	CFh	Frequency control for PWM2
x	LUT 1 Base Temperature	D0h	Base temperature to which look-up table offset is applied for LUT 1
x	LUT 2 Base Temperature	D1h	Base temperature to which look-up table offset is applied for LUT 2
x	LUT 3 Base Temperature	D2h	Base temperature to which look-up table offset is applied for LUT 3
x	LUT 4 Base Temperature	D3h	Base temperature to which look-up table offset is applied for LUT 4
x	Step 2 Temp Offset	D4h	Step 2 LUT 1/2 and LUT 3/4 Offset Temperatures
x	Step 3 Temp Offset	D5h	Step 3 LUT 1/2 and LUT 3/4 Offset Temperatures
x	Step 4 Temp Offset	D6h	Step 4 LUT 1/2 and LUT 3/4 Offset Temperatures
x	Step 5 Temp Offset	D7h	Step 5 LUT 1/2 and LUT 3/4 Offset Temperatures

13.0 Registers (Continued)

Lock	Register Name	Address	Description
SETUP REGISTERS			
x	Step 6 Temp Offset	D8h	Step 6 LUT 1/2 and LUT 3/4 Offset Temperatures
x	Step 7 Temp Offset	D9h	Step 7 LUT 1/2 and LUT 3/4 Offset Temperatures
x	Step 8 Temp Offset	DAh	Step 8 LUT 1/2 and LUT 3/4 Offset Temperatures
x	Step 9 Temp Offset	DBh	Step 9 LUT 1/2 and LUT 3/4 Offset Temperatures
x	Step 10 Temp Offset	DCh	Step 10 LUT 1/2 and LUT 3/4 Offset Temperatures
x	Step 11 Temp Offset	DDh	Step 11 LUT 1/2 and LUT 3/4 Offset Temperatures
x	Step 12 Temp Offset	DEh	Step 12 LUT 1/2 and LUT 3/4 Offset Temperatures
x	Step 13 Temp Offset	DFh	Step 13 LUT 1/2 and LUT 3/4 Offset Temperatures
	TACH to PWM Binding	E0h	Controls the tachometer input to PWM output binding
x	Tach Boost Control	E1h	Controls the fan boost function upon a tach error
x	LM94 Status/Control	E2h	Gives Master error status, ASF reset control and Max PWM control
x	LM94 Configuration	E3h	Configures various outputs and provides START bit
SLEEP STATE CONTROL AND MASK REGISTERS			
	Sleep State Control	E4h	Used to communicate the system sleep state to the LM94
	S1 GPI Mask	E5h	Sleep state S1 GPI error mask register
	S1 Fan Mask	E6h	Sleep state S1 fan tach error mask register
	S3 GPI Mask	E7h	Sleep state S3 GPI error mask register
	S3 Fan Mask	E8h	Sleep state S3 fan tach error mask register
	S3 Temperature/Voltage Mask	E9h	Sleep state S3 temperature or voltage error mask register
	S4/5 GPI Mask	EAh	Sleep state S4/5 GPI error mask register
	S4/5 Temperature/Voltage Mask	EBh	Sleep state S4/5 temperature or voltage error mask register
OTHER MASK REGISTERS			
	GPI Error Mask	ECh	Error mask register for GPI faults
	Miscellaneous Error Mask	EDh	Error mask register for $\overline{\text{VRDx\_HOT}}$, $\overline{\text{GPI}}$, and dynamic Vccp limit checking.
ZONE 1a AND 2a TEMPERATURE READING ADJUSTMENT REGISTERS			
	Zone 1a Temp Adjust	EEh	Allows all Zone 1a temperature measurements to be adjusted by a programmable offset
	Zone 2a Temp Adjust	EFh	Allows all Zone 2a temperature measurements to be adjusted by a programmable offset
BLOCK COMMANDS			
	Block Write Command	F0h	SMBus Block Write Command Code
	Block Read Command	F1h	SMBus Block Write/Read Process call
	Fixed Block 0	F2h	Fixed block code address 40h, size 8 bytes
	Fixed Block 1	F3h	Fixed block code address 48h, size 8 bytes
	Fixed Block 2	F4h	Fixed block code address 50h, size 6 bytes
	Fixed Block 3	F5h	Fixed block code address 56h, size 16 bytes
	Fixed Block 4	F6h	Fixed block code address 67h, size 4 bytes
	Fixed Block 5	F7h	Fixed block code address 6Eh, size 8 bytes
	Fixed Block 6	F8h	Fixed block code address 78h, size 12 bytes
	Fixed Block 7	F9h	Fixed block code address 90h, size 32 bytes
	Fixed Block 8	FAh	Fixed block code address B4h, size 8 bytes
	Fixed Block 9	FBh	Fixed block code address C8h, size 8 bytes
	Fixed Block 10	FCh	Fixed block code address D0h, size 16 bytes

13.0 Registers (Continued)

Lock	Register Name	Address	Description
BLOCK COMMANDS			
	Fixed Block 11	FDh	Fixed block code address E5h, size 9 bytes
	Reserved	FEh-FFh	Reserved for future commands

Please contact your local sales office for complete LM94 applications information.

14.0 Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Positive Supply Voltage (V_{DD})	6.0V
Voltage on Any Digital Input or Output Pin	−0.3V to 6.0V (Except Analog Inputs)
Voltage on +5V Input	−0.3V to +6.667V
Voltage at Positive Remote Diode Inputs, AD_IN1, AD_IN2, AD_IN3, and AD_IN15 Inputs	−0.3V to (V_{DD} + 0.05V)
Voltage at Other Analog Voltage Inputs	−0.3V to +6.0V
Input Current at Thermal Diode Negative Inputs	±1 mA
Input Current at any pin (Note 3)	±10mA
Package Input Current (Note 3)	±100 mA
Maximum Junction Temperature (Note 9) (T_{JMAX})	150 ˚C
ESD Susceptibility (Note 4)	
Human Body Model	3 kV
Machine Model	300V
Charged Device Model	750V
Storage Temperature	−65˚C to +150˚C

Soldering process must comply with National's reflow temperature profile specifications. Refer to www.national.com/packaging/. (Note 5)

15.0 Operating Ratings (Notes 1, 2)

	$T_{MIN} \le T_A \le T_{MAX}$
Operating Temperature Range	0˚C ≤ T_A ≤ +85˚C
Nominal Supply Voltage	3.3V
Supply Voltage Range (V_{DD})	+3.0V to +3.6V
VID0-VID5	−0.05V to +5.5V
Digital Input Voltage Range	−0.05V to (V_{DD} + 0.05V)
Package Thermal Resistance (Note 6)	79˚C/W

DC Electrical Characteristics

The following limits apply for +3.0 V_{DC} to +3.6 V_{DC}, unless otherwise noted. **Bold face limits apply for $T_A = T_J$ over T_{MIN} to T_{MAX} of the operating range;** all other limits $T_A = T_J$ = 25˚C unless otherwise noted. T_A is the ambient temperature of the LM94; T_J is the junction temperature of the LM94; T_D is the junction temperature of the thermal diode.

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 10)	Units (Limits)
POWER SUPPLY CHARACTERISTICS					
	Power Supply Current	Converting, Interface and Fans Inactive, Peak Current	2	**2.75**	mA (max)
		Converting, Interface and Fans Inactive, Average Current	1.6		mA
	Power-On Reset Threshold Voltage		2	**1.6**	V (min)
				2.7	V (max)
TEMPERATURE-TO-DIGITAL CONVERTER CHARACTERISTICS					
	Local Temperature Accuracy Over Full Range	0˚C ≤ T_A ≤ 85˚C	±2	**±3**	˚C (max)
		T_A = +55˚C	±1	**±2.5**	˚C (max)
	Local Temperature Resolution		1		˚C
	Remote Thermal Diode Temperature Accuracy Over Full Range; targeted for a typical Pentium processor on 90 nm or 65 nm process(Note 8)	0˚C ≤ T_A ≤ 85˚C and 0˚C ≤ T_D ≤ 100˚C		**±3**	˚C (max)
		0˚C ≤ T_A ≤ 85˚C and T_D =70˚C		**±2.5**	˚C (max)
	Remote Thermal Diode Temperature Accuracy; targeted for a typical Pentium processor on 90nm or 65nm process (Note 8)	0˚C ≤ T_A ≤ 85˚C and 25˚C ≤ T_D ≤ 70˚C	±1		˚C
	Remote Temperature Resolution		1		˚C
	Thermal Diode Source Current	High Level	172	**230**	µA (max)
		Low Level	10.75		µA
	Thermal Diode Current Ratio		16		
T_C	Total Monitoring Cycle Time			**100**	ms (max)

DC Electrical Characteristics (Continued)

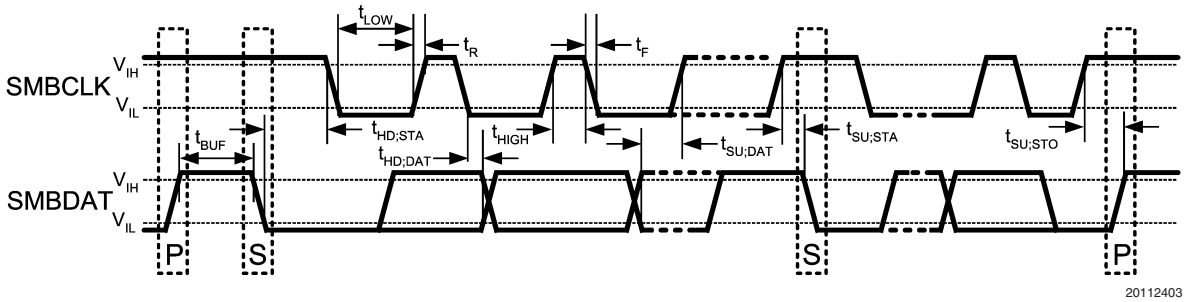
The following limits apply for +3.0 V_{DC} to +3.6 V_{DC}, unless otherwise noted. **Bold face limits apply for $T_A = T_J$ over T_{MIN} to T_{MAX} of the operating range;** all other limits $T_A = T_J = 25^{\circ}C$ unless otherwise noted. T_A is the ambient temperature of the LM94; T_J is the junction temperature of the LM94; T_D is the junction temperature of the thermal diode.

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 10)	Units (Limits)
ANALOG-TO-DIGITAL VOLTAGE MEASUREMENT CONVERTER CHARACTERISTICS					
TUE	Total Unadjusted Error (Note 12)			**±2**	% of FS (max)
DNL	Differential Non-Linearity		±1		LSB
PSS	Power Supply (V_{DD}) Sensitivity		±1		%/V (of FS)
T_C	Total Monitoring Cycle Time			**100**	ms (max)
	Input Resistance for Inputs with Dividers		200	**140**	kΩ (min)
	AD_IN1- AD_IN3 and AD_IN15 Analog Input Leakage Current (Note 13)			60	nA (max)
REFERENCE OUTPUT (V_{REF}) CHARACTERISTICS					
	Tolerance			**±1**	% (max)
V_{REF}	Output Voltage (Note 14)		2.500	**2.525** **2.475**	V (max) V (min)
	Load Regulation	I_{SOURCE} = −2 mA I_{SINK} = 2 mA	0.1		%
DIGITAL OUTPUTS: PWM1, PWM2					
I_{OL}	Maximum Current Sink			**8**	mA (min)
V_{OL}	Output Low Voltage	I_{OUT} = 8.0 mA		**0.4**	V (max)
DIGITAL OUTPUTS: ALL					
V_{OL}	Output Low Voltage (Note excessive current flow causes self-heating and degrades the internal temperature accuracy.)	I_{OUT} = 4.0 mA		**0.4**	V (min)
		I_{OUT} = 6 mA		**0.55**	V (min)
I_{OH}	High Level Output Leakage Current	$V_{OUT} = V_{DD}$	0.1	**10**	µA (max)
I_{OTMAX}	Maximum Total Sink Current for all Digital Outputs Combined			**32**	mA (max)
C_O	Digital Output Capacitance		20		pF
DIGITAL INPUTS: ALL					
V_{IH}	Input High Voltage Except Address Select			**2.1**	V (min)
V_{IL}	Input Low Voltage Except Address Select			**0.8**	V (max)
V_{IH}	Input High Voltage for Address Select			**90% V_{DD}**	V (min)
V_{IM}	Input Mid Voltage for Address Select			**43% V_{DD}** **57% V_{DD}**	V (min) V (max)
V_{IL}	Input Low Voltage for Address Select			**10% V_{DD}**	V (max)
V_{HYST}	DC Hysteresis		0.3		V
I_{IH}	Input High Current	$V_{IN} = V_{DD}$		**−10**	µA (min)
I_{IL}	Input Low Current	V_{IN} = 0V		**10**	µA (max)
C_{IN}	Digital Input Capacitance		20		pF
DIGITAL INPUTS: P1_VIDx, P2_VIDx, GPI_9, GPI_8, GPIO_7, GPIO_6, GPIO_5, GPIO_4 (When respective bit set in Register BEh GPI/VID Level Control)					
V_{IH}	Alternate Input High Voltage (AGTL+ Compatible)			**0.8**	V (min)
V_{IL}	Alternate Input Low Voltage (AGTL+ Compatible)			**0.4**	V (max)

AC Electrical Characteristics

The following limits apply for +3.0 V_{DC} to +3.6 V_{DC}, unless otherwise noted. **Bold face limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX} of the operating range;** all other limits $T_A = T_J = 25^{\circ}C$ unless otherwise noted.

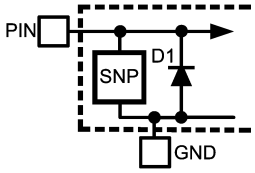
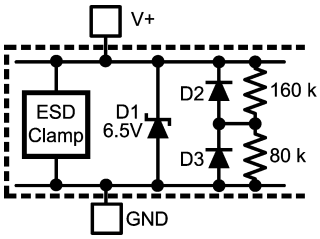
Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 10)	Units (Limits)
FAN RPM-TO-DIGITAL CHARACTERISTICS					
	Counter Resolution		14		bits
	Number of fan tach pulses count is based on		2		pulses
	Counter Frequency		22.5		kHz
	Accuracy			**±6**	% (max)
PWM OUTPUT CHARACTERISTICS					
	Frequency Tolerances			**±6**	% (max)
	Duty-Cycle Tolerance		±2	**±6**	% (max)
RESET INPUT/OUTPUT CHARACTERISTICS					
	Output Pulse Width Upon Power Up			**250** **330**	ms (min) ms (max)
	Minimum Input Pulse Width			**10**	µs (min)
	Reset Output Fall Time	1.6V to 0.4V Logic Levels		**1**	µs (max)
SMBus TIMING CHARACTERISTICS					
f_{SMBCLK}	SMBCLK (Clock) Clock Frequency			**10** **100**	kHz (min) kHz (max)
t_{BUF}	SMBus Free Time between Stop and Start Conditions			**4.7**	µs (min)
$t_{HD;STA}$	Hold time after (Repeated) Start Condition. After this period, the first clock is generated.			**4.0**	µs (min)
$t_{SU;STA}$	Repeated Start Condition Setup Time			**4.7**	µs (min)
$t_{SU;STO}$	Stop Condition Setup Time			**4.0**	µs (min)
$t_{SU;DAT}$	Data Input Setup Time to SMBCLK High			**250**	ns (min)
$t_{HD;DAT}$	Data Output Hold Time after SMBCLK Low			**300** **1075**	ns (min) ns (max)
t_{LOW}	SMBCLK Low Period			**4.7** **50**	µs (min) µs (max)
t_{HIGH}	SMBCLK High Period			**4.0** **50**	µs (min) µs (max)
t_R	Rise Time			**1**	µs (max)
t_F	Fall Time			**300**	ns (max)
$t_{TIMEOUT}$	Timeout SMBDAT or SMBCLK low time required to reset the Serial Bus Interface to the Idle State		31	 **25** **35**	ms ms (min) ms (max)
t_{POR}	Time in which a device must be operational after power-on reset	V_{DD} > +2.8V		**500**	ms (max)
C_L	Capacitance Load on SMBCLK and SMBDAT			**400**	pF (max)



Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

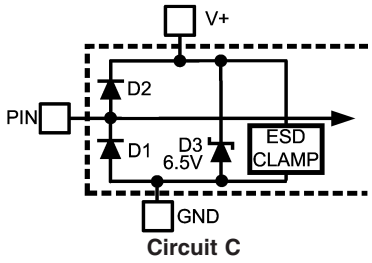
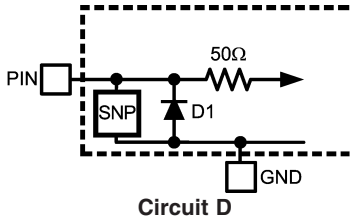
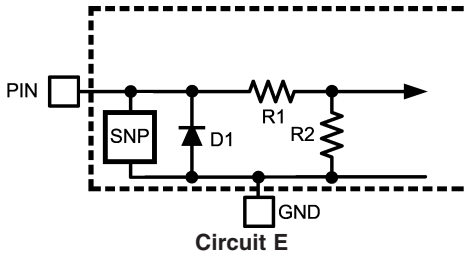
Note 2: All voltages are measured with respect to GND, unless otherwise noted.

Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supplies (V_{IN} < (GND or AGND) or V_{IN} > V_{DD}, except for analog voltage inputs), the current at that pin should be limited to 10 mA. The 100 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 10 mA to ten. Parasitic components and/or ESD protection circuitry are shown below for the LM94's pins. Care should be taken not to forward bias the parasitic diode, D1, present on pins D+ and D– as shown in circuits C and D. Doing so by more than 50 mV may corrupt temperature measurements. D1 and the ESD Clamp are connected between V+ (V_{DD}, AD_IN16) and GND as shown in circuit B. SNP stands for snap-back device.

Symbol	Pin #	Circuit	All Input Circuits
GPIO_0/TACH1	1	A	
GPIO_1/TACH2	2	A	
GPIO_2/TACH3	3	A	
GPIO_3/TACH4	4	A	
GPIO_4 / $\overline{\text{P1\_THERMTRIP}}$	5	A	
GPIO_5 / $\overline{\text{P2\_THERMTRIP}}$	6	A	
GPIO_6	7	A	
GPIO_7	8	A	
$\overline{\text{VRD1\_HOT}}$	9	A	
$\overline{\text{VRD2\_HOT}}$	10	A	
$\overline{\text{SCSI\_TERM1}}$	11	A	
$\overline{\text{SCSI\_TERM2}}$	12	A	
SMBDAT	13	A	
SMBCLK	14	A	
$\overline{\text{ALERT}}$/XtestOut	15	A	
$\overline{\text{RESET}}$	16	A	
AGND	17	B (Internally shorted to GND pin.)	
V_{REF}	18	A	
REMOTE1–	19	C	
REMOTE1+	20	D	
REMOTE2–	21	C	
REMOTE+	22	D	

Circuit A

Circuit B

Symbol	Pin #	Circuit	All Input Circuits
AD_IN1	23	D	
AD_IN2	24	D	
AD_IN3	25	D	
AD_IN4	26	E	
AD_IN5	27	E	
AD_IN6	28	E	
AD_IN7	29	E	
AD_IN8	30	E	
AD_IN9	31	E	
AD_IN10	32	E	
AD_IN11	33	E	
AD_IN12	34	E	
AD_IN13	35	E	
AD_IN14	36	E	
AD_IN15	37	D	
ADDR_SEL	38	A	
AD_IN16/V_{DD} (V+)	39	B	
GND	40	B (Internally shorted to AGND.)	
PWM1	41	A	
PWM2	42	A	
P1_VID0	43	A	
P1_VID1	44	A	
P1_VID2	45	A	
P1_VID3	46	A	
P1_VID4	47	A	
P1_VID5	48	A	
$\overline{\text{P1\_PROCHOT}}$	49	A	
$\overline{\text{P2\_PROCHOT}}$	50	A	
P2_VID0	51	A	
P2_VID1	52	A	
P2_VID2	53	A	
P2_VID3	54	A	
P2_VID4	55	A	
P2_VID5	56	A	

Circuit C

Circuit D

Circuit E

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor. Machine model, 200 pF discharged directly into each pin. Charged device model (CDM) simulates a pin slowly acquiring charge (such as from a device sliding down the feeder in an automated assembler) then rapidly being discharged.

Note 5: Reflow temperature profiles are different for lead-free and non lead-free packages.

Note 6: The maximum power dissipation must be de-rated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_{D\ MAX} = (T_{JMAX} - T_A) / \theta_{JA}$. The θ_{JA} for the LM94 when mounted to 1 oz. copper foil PCB the θ_{JA} with different air flow is listed in the following table.

Air Flow	Junction to Ambient Thermal Resistance, θ_{JA}
0 m/s	79 ˚C/W
1.14 m/s (225 LFPM)	62 ˚C/W
2.54 m/s (500 LFPM)	52 ˚C/W

Note 7: See the URL "http://www.national.com/packaging/" for other recommendations and methods of soldering surface mount devices.

Note 8: At the time of first pubication of this specification (Jan 2006), this specification applies to either Pentium or Xeon Processors on 90nm or 65nm process when TruTherm is selected. When TruTherm is deselected this specification applies to an MMBT3904. This specification does include the error caused by the variability of the diode ideality and series resistance parameters.

Note 9: Typical parameters are at $T_J = T_A = 25$ ˚C and represent most likely parametric norm.

Note 10: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 11: TUE (Total Unadjusted Error) includes Offset, Gain and Linearity errors of the ADC.

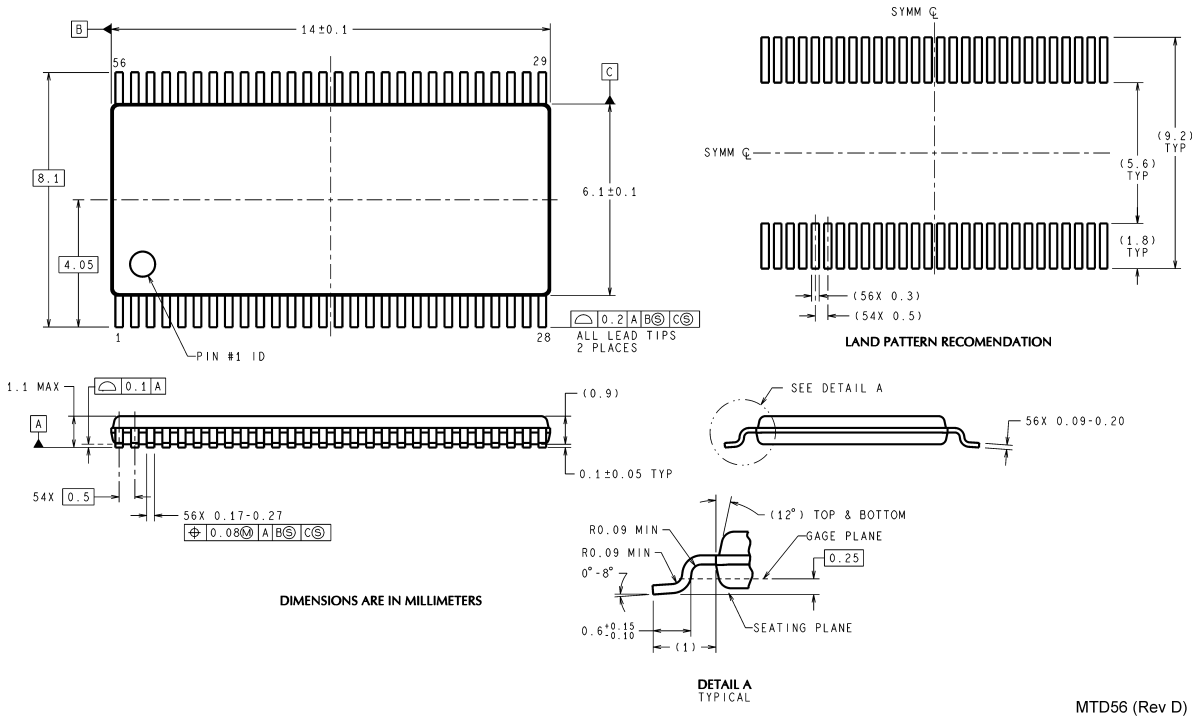
Note 12: Total Monitoring Cycle Time includes all temperature and voltage conversions.

Note 13: Leakage current approximately doubles every 20 ˚C.

Note 14: A total digital I/O current of 40 mA can cause 6 mV of offset in Vref.

Note 15: Timing specifications are tested at the TTL logic levels, V_{IL} = 0.4V for a falling edge and V_{IH} = 2.4V for a rising edge. TRI-STATE output voltage is forced to 1.4V.

16.0 Physical Dimensions inches (millimeters) unless otherwise noted



MTD56 (Rev D)

56-Lead Molded TSSOP Package,
JEDEC Registration Number MO-153 Variation EE,
Order Number LM94CIMT or LM94CIMTX,
NS Package Number MTD56

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